NOTE: This page is for information only. It's been many years since anyone has been active on this group project.

These are my preliminary design notes for the prototype CPCNG computer. The official CPCNG website (http://cpcng.free.fr) no longer exists. It used to contain a complete description of what the CPCNG computer is, why we are building it, the operating system, the applications software and the current state of the project. The descriptions and diagrams on this page are intended as a basis for discussion and a guide for the developer of the FPGA which will form the backbone of the prototype. Additionally they will provide a precise specification of the prototype hardware, I/O map and memory map for the group developing the emulator.

Prototype Board Contents

The prototype board will contain the following components:

1. eZ80 CPU from Zilog
2. 128K EEPROM
3. 128K Fast SRAM for video and CPC-mode
4. FPGA containing IDE hard drive interface , video, memory mapping and CPC-compatibility logic
5. Sockets for large PC-style SDRAM cards
6. Sockets for modem, keyboard, mouse and power supply
7. Expansion sockets for new cards to be designed later

Block Diagram

A simplified block diagram of the prototype is shown below. This shows the interconnection of the various units discussed below and it will be apparent that most of the units will be coded in the FPGA. This diagram does not show the control signals (WR/RD/IOREQ etc.) which would overcomplicate the diagram at this level.

{gallery}cpcng{/gallery}

CPU

We will use an eZ80 CPU. A supplier has been located (WBC Europe), who are willing to

provide them in small quantities at a price of £9.93 each (approx USD 14, EUR 16, FRF 105, DEM 31). The eZ80 actually comes as the eZ80190 Webserver, which is an eZ80 core plus various on-chip timers and interfaces. This chip is now available (Oct-01) but since it is new there is a lead time of some 2 months according to WBC.

Memory

We will use PC-type SDRAM cards for the main memory. A 128K fast SRAM will also be used as video RAM and in the CPC compatibility mode. A 128K ROM (EPROM or EEPROM) will contain boot code and any other required code e.g. the old CPC ROM's for the compatibility mode. The eZ80 address space is 16M, and the large SDRAM will be mapped in up to 256 4M blocks giving a total capacity of up to 1G. The 128K video RAM and 128K ROM will be mapped at programmable locations. Click here for a detailed description of the memory mapping.

CPC Compatibility

The CPCNG will have a CPC mode where it will be able to run CPC software without modification. Software which relies on precise timing (e.g. demos) may not work as expected since the eZ80 is much faster than the old Z80, and certain software emulation of CPC hardware will be required. I have designed a draft circuit diagram for the CPC I/O intercept unit, with a detailed description: Read more...

Peripherals

The CPCNG will initially use PC-compatible peripherals. These are readily available and cheap, or even free where they can be salvaged from surplus or salvaged obsolete PC's. The peripherals used will be:

1. PC power supply
2. PC keyboard (AT)
3. PC IDE hard disk
4. PC mouse
5. VGA compatible monitor

Click here for more information about the IDE hard disk interface.

The keyboard interface will be initially (in the prototype) just a connection to I/O pins on the eZ80 which will manage the keyboard serial interface in software. Similarly the mouse socket will just be connected to eZ80 I/O pins. A modem socket will also be connected to eZ80 I/O pins, as certain eZ80 I/O ports are designed to be able to connect to a modem. Later keyboard and mouse interfaces can be designed in the FPGA, but in the prototype to keep the hardware as simple as possible, these interfaces will be managed in software by the eZ80 and its onboard

I/O ports.

PCB

The prototype PCB will be produced in a small quantity, perhaps by a supplier such as Express PCB .
It will contain the eZ80, 128K ROM, 128K SRAM, FPGA and sockets for: modem, keyboard, IDE hard disk, mouse, VGA monitor, power supply, SDRAM (PC cards) and several expansion sockets for further developments.

FPGA

A large Field Programmable Gate Array (FPGA) will be used to implement all of the logic in the CPCNG, including the video circuit, IDE hard drive interface, memory mapping and CPC compatibility unit. The availability of FPGA's is a major advantage to us as it allows the use of complex logic circuits while minimising the chipcount, thus making the computer cheap and easily constructed by the group members.

There has been no final choice of FPGA but Xilinx seems to be the popular choice. My suggestion is to use schematic entry where possible because this will be most easily understood by the majority of people. Various cheap Xilinx development boards can be found (e.g. by XESS) but my suggestion is that we put the FPGA directly on the board, with a JTAG programming socket and do development directly on the CPCNG prototype board using PC FPGA development tools.

The following summarises the circuit blocks which will exist in the FPGA.

1. CRTC Video driver: For CPC compatibility we intend to use the 6845. This will be implemented in the FPGA, from a free VHDL model for the 6845 which is available from Opencores
. The 6845 will use the 128K SRAM, and arbitration of this memory between the eZ80 and the 6845 will also be managed by logic in the FPGA. More on this much-discussed topic later!

2. IDE interface: A simple interface with latches for the upper 8-bits of the 16-bit IDE bus. Click here
for more information about the IDE hard disk interface.

3. Memory mapping unit: maps SDRAM in 4M blocks. Also does mapping in the CPC mode in 16K blocks, as on an old CPC. Click here for a detailed description of the memory mapping.

4. SDRAM controller: possibly using VHDL from Opencores .

5. CPC I/O intercept trick: To obtain maximum CPC compatibility, all I/O requests in CPC mode are intercepted by the FPGA and create a non-maskable interrupt. A routine at &0066 (NMI call address) translates the CPC I/O attempted, does the appropriate CPCNG thing, and puts the eZ80 registers in the state the CPC would have expected. I have designed a draft circuit diagram for the CPC I/O intercept unit, with a detailed description.
Read more...

6. Video RAM arbitration unit: Switches the 128K fast SRAM between the eZ80 and the 6845 CRTC.

Future Versions

Future versions of the CPCNG will include an advanced graphics processor and sound capabilities. The prototype described here deliberately omits these in an effort to minimise complexity. We need a prototype which is simple enough to be achievable, yet capable of expansion and operating as a test bed for the future verions. It is anticipated that once the CPCNG prototype board is working, a number will be built by members of the group, and hardware development will then expand. Different groups will be able to work on different sections of the hardware for the next version.