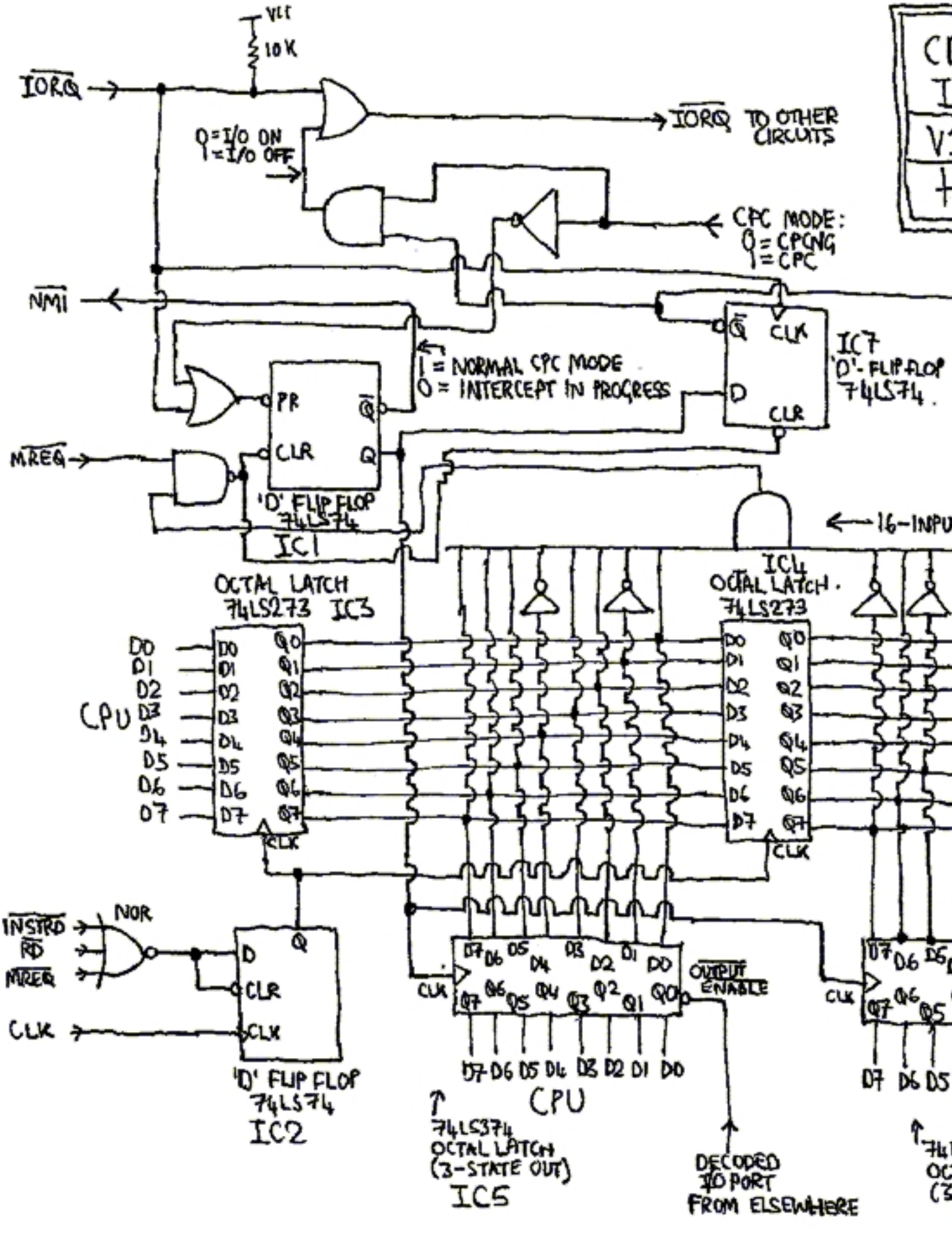
This is a draft design for the CPC-compatibility circuit. This logic will reside in the FPGA, and will equip the CPCNG with e CPC-compatibility mode in which almost all old CPC software will run. Exceptions will be anything which makes use of precise timing, since the eZ80 runs at a totally different pace to the old Z80, the video memory arbitration is organised differently in the CPCNG, and there is an extra overhead associated with translation and emulation of CPC I/O.

Refer to the below diagram of the CPC-compatibility circuit. If we use schematic entry for the FPGA we can enter this circuit for the I/O intercept trick. I have marked the main chips in this design with equivalent TTL 74LS-series part numbers, just so that their functionality is well defined (in reality 74LS logic would be too slow to be able to build his circuit for real).


VCC
10K
IORQ
Q=I/O ON
1=I/O OFF
IORQ TO OTHER CIRCUITS
CPC MODE:
0=CPCNG
1=CPC
NMI
1=NORMAL CPC MODE
0=INTERCEPT IN PROGRESS
IC7
'D'-FLIP FLOP
74LS74
PR
CLR
'D' FLIP FLOP
74LS74
IC1
MREQ
16-INPU
OCTAL LATCH
74LS273 IC3
IC4
OCTAL LATCH
74LS273
CPU
D0
D1
D2
D3
D4
D5
D6
D7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CLK
INSTRD
RD
MREQ
NOR
CLK
'D' FLIP FLOP
74LS74
IC2
OUTPUT ENABLE
74LS374
OCTAL LATCH
(3-STATE OUT)
IC5
DECODED
IO PORT
FROM ELSEWHERE