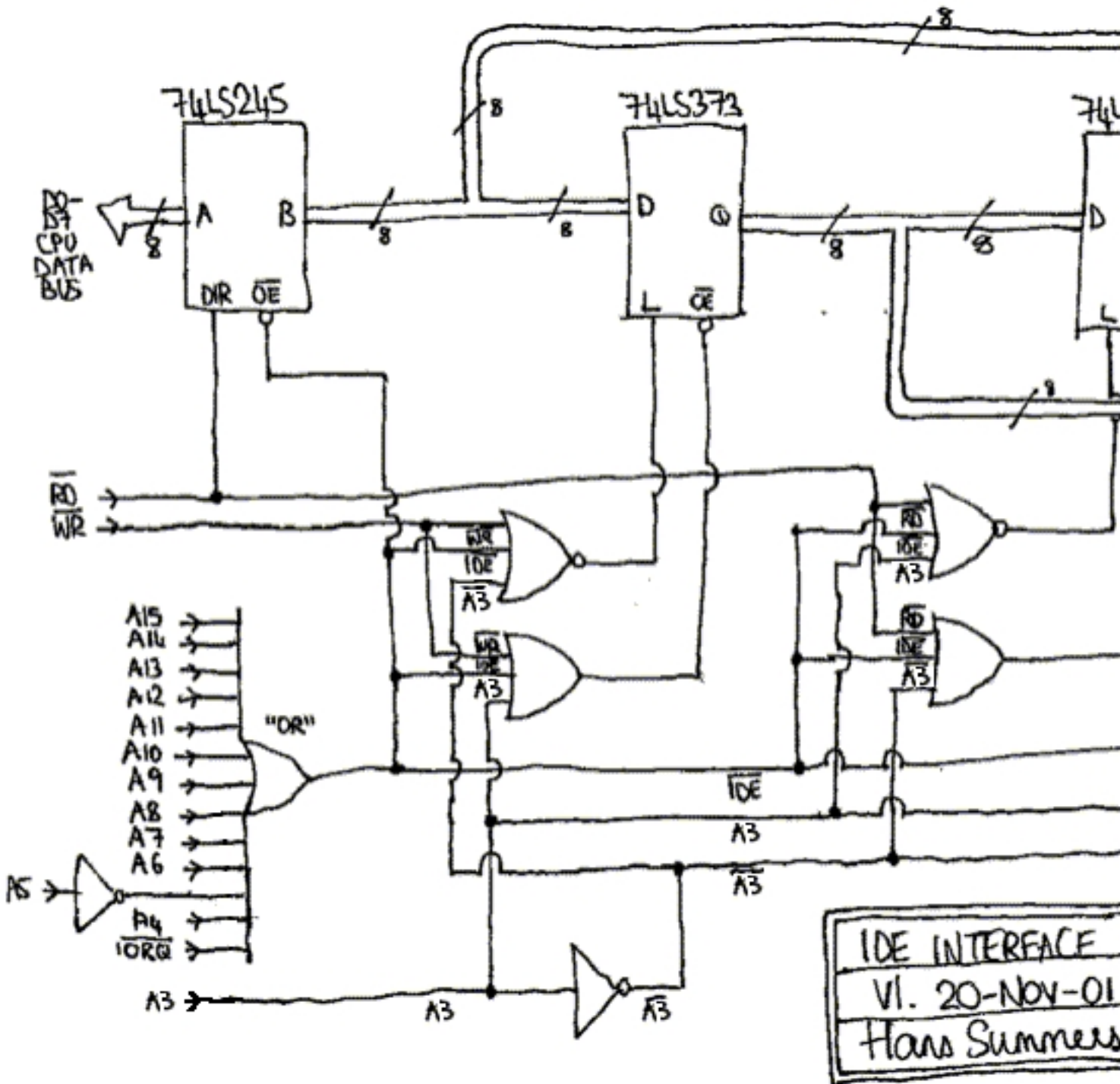


CPCNG Notes: IDE interface

Written by Hans Summers
Monday, 25 January 2010 20:04 -

This page describes the proposed IDE hard disk interface. The IDE specification is simpler than SCSI so has been chosen for the prototype. The IDE interface would be almost trivial but for the fact that the IDE databus is 16 bits wide, whereas the eZ80 data bus is only 8 bits wide. It is possible to connect only 8 bits of the IDE bus directly to the eZ80 data bus, but doing this sacrifices half the capacity of the disk drive.

The solution here is to buffer the high byte of the data word in an 8-bit latch, which is read/written to on an additional port number. There are a number of examples of this on the internet, with circuit diagrams and sample code (see list of links below). The information and circuit described here are derived from these project pages. Below is the draft circuit diagram.



CPC NG I/O Addresses for IDE Registers

The following table describes the port mapping of the IDE interface:

Port	Register	Function
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CPCNG Notes: IDE interface

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&0020	IDELO	Data Port (low byte)
&0021	IDEERR	Read: Error Register; Write: Precomp
&0022	IDESECTC	Sector Count
&0023	IDESECTN	Sector Number
&0024	IDECYLLO	Cylinder Low
&0025	IDECYLHI	Cylinder High
&0026	IDEHEAD	Drive/Head
&0027	IDESTTS	Read: Status; Write: Command
&0028	IDEHI	Data Port (High Byte)
&0029		
Not Used		
&002A		
Not Used		
&002B		
Not Used		
&002C		
Not Used		

CPCNG Notes: IDE interface

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Monday, 25 January 2010 20:04 -

&002D		
Not Used		
&002E	IDECTRL	Read: Alternative Status; Write; Device Control
&002F	IDEADDR	Drive Address (Read Only)

IDE Project Links

These are links to IDE projects with circuit diagrams, information, sample code and more.

- <http://www.gaby.de/gide/> All about the GIDE interface
- http://home.freiepresse.de/befis/hdif_e.htm ZX81 Harddisc
- <http://members.lycos.co.uk/leedavison/6502/ide/index.html> IDE bus interface circuit
- <http://8bs.aussie.nu/subide.htm> BBC IDE interface
- <http://home.hccnet.nl/g.baltissen/ide.htm> IDE interface for the Commodore 64/128
- <http://www.pjrc.com/tech/8051/ide/> 8051 IDE Hard Drive Interface
- <http://www.students.tut.fi/~leinone3/ide.html> IDE Harddisk project for the Amiga 500
- <http://blkbox.com/~jdbaker/SmallSys/8bitIDE.html> IDE Devices on 8-bit machines
- <http://www.angelfire.com/wa2/ratgod/odcp/data.html> IDE Project
- <http://home.freeuk.net/c.ward/6502/index.html> Chirs Ward's 6502 Computer system (incl IDE)
- <http://members.tripod.com/~piters/zx.htm> Spectrum Hardware DIY: IDE interface
- <http://sorry.vse.cz/~xrihp01/specocy/hardware/zxide/> Spectrum IDE interface (in Czechoslovakian)
- <http://www.icon.co.za/~dantohi/> 48K ZX Spectrum expansion system
- http://members.freemail.absa.co.za/dan_antohi/ 48K ZX Spectrum expansion system (mirror)

IDE Register descriptions

This section describes the IDE register usage.

&0021 (write): Write Precomp: A write to this port sets the "Write Precompensation Cylinder divided by 4". Not sure what this means.

&0021 (read): Error Register: The contents of the error register when in diagnostic mode are shown in this table:

CPCNG Notes: IDE interface

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Value	Error
1	No Error detected
2	Formatter device error
3	Sector buffer error
4	ECC circuitry error
5	Controlling microprocessor error

The contents of the error register (read &0021) when in operation mode are shown in this table:

Bit	Value	Meaning
0	0	DAM found

CPCNG Notes: IDE interface

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Monday, 25 January 2010 20:04 -

1	DAM not found	
1	0	Track 000 found

1	Track 000 not found	
2	0	Command completed

1	Command aborted	
3	0	Reserved
4	0	ID found

1	ID not found	
5	0	Reserved
6	0	No error

1	Uncorrectable ECC error	
7	0	Block OK

CPCNG Notes: IDE interface

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Monday, 25 January 2010 20:04 -

1	Bad Block detected
---	--------------------

&0026: Drive/Head: Bit 4 of the drive/head register selects drive 0 or drive 1, and bits 3-0

select the head.

&0027 (read): Status: Bits in the status register are set to 1 to indicate one of the following

conditions:

Bit	Condition
0	Previous command ended in an error
1	Index: set to 1 each disk revolution

CPCNG Notes: IDE interface

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Monday, 25 January 2010 20:04 -

2	Disk data read successfully corrected
3	Sector buffer requires servicing
4	Seek complete
5	Write fault
6	Drive is ready
7	Controller is executing a command

&0027 (write): Command: Writes to the command register are as follows:

Command	Function
98 E5	check power mode (IDE)
90	execute drive diagnostics

CPCNG Notes: IDE interface

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Monday, 25 January 2010 20:04 -

50	format track
EC	identify drive (IDE)
97 E3	idle (IDE)
95 E1	idle immediate (IDE)
91	initialise drive parameters
1x	recalibrate
E4	read buffer (IDE)
C8	read DMA with retry (IDE)
C9	read DMA without retry (IDE)
C4	read multiples (IDE)
20	read sectors with retry
21	read sectors without retry
22	read long with retry
23	read long without retry
40	read verify sectors with retry
41	read verify sectors without retry
7x	seek

CPCNG Notes: IDE interface

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Monday, 25 January 2010 20:04 -

EF	set features (IDE)
C6	set multiple mode (IDE)
99 E6	set sleep mode (IDE)
96 E2	standby (IDE)
94 E0	standby immediate (IDE)
E8	write buffer (IDE)
CA	write DMA with retry (IDE)
CB	write DMA with retry (IDE)
C5	write multiple (IDE)
E9	write same (IDE)
30	write sectors with retry
31	write sectors without retry
32	write long with retry
33	write long without retry
3C	write verify (IDE)
9A	vendor unique (IDE)
C0-C3	vendor unique (IDE)

CPCNG Notes: IDE interface

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8x	vendor unique (IDE)
F0-F4	EATA standard (IDE)
F5-FF	vendor unique (IDE)